Automatic Assembly for Microelectronic Components

Zeungnam Bien, Sang-Rok Oh, Il Hong Suh, Jae Ok Kim, and Young Seok Oh

ABSTRACT: This paper describes the design and development of an automatic assembly machine for microelectronic components. The machine uses multiple microprocessors to accomplish its tasks, which include process supervision, visual pattern recognition, and information display. The control system was implemented in real time on a laboratory semiconductor die bonding machine.

Introduction

Machines for automatic assembly of microelectronic components, such as semiconductor die bonding machines, are complex systems equipped with sophisticated sensors, such as TV cameras and sophisticated actuators, e.g., mechanical manipulators. The design of such machines requires a control system that integrates visual pattern recognition, guidance of components, control for mechanical manipulators, and sequential control of mechanical fixturing devices and material transport [1], [2].

This paper describes the design of a multiprocessor-based automatic semiconductor die bonding machine. The mechanical structure of the machine is based on operating functions similar to those of existing machines [3]. The electronic control system is designed to be a master-slave type consisting of three subsystems, each of which employs a 16-bit microprocessor, the MC68000. A special feature is that the system is fully automatic; manual operation is minimized by means of automatic measurements of size and orientation of components with subsequent automatic corrections. In particular, the structured supervisory controller works as a real-time operating system for the multiprocessors, with multitask control, and effectively coordinates all sensor signals and actuator functions. Also, various image processing algorithms are incorporated into the control system for fast and reliable operation by employing on-line processing units and a real-time frame grabber.

Overall System Configuration

The semiconductor die bonding machine presented here is a typical automatic assembly machine for microelectronic components, as shown in Fig. 1. The mechanical aspects of this assembly machine consist of the following three modules: (1) bonding head module, (2) wafer feeding module, and (3) lead frame feeding module.

The bonding head module is constructed by using two step motors and two DC motors as actuators and is utilized to transfer each die from a wafer to a sequence of lead frames. The plunge-up unit is also included in this module, which is actuated by a step motor and utilized to push up each die when the bonding head picks up a die.

The wafer feeding module consists of a camera with a microscope for inspection and measurements of position of transferred die, an *XY* table driven by two step motors for wafer feeding, a jig holder actuated by a step motor, and a wafer loader and unloader.

Finally, the lead frame feeding module is

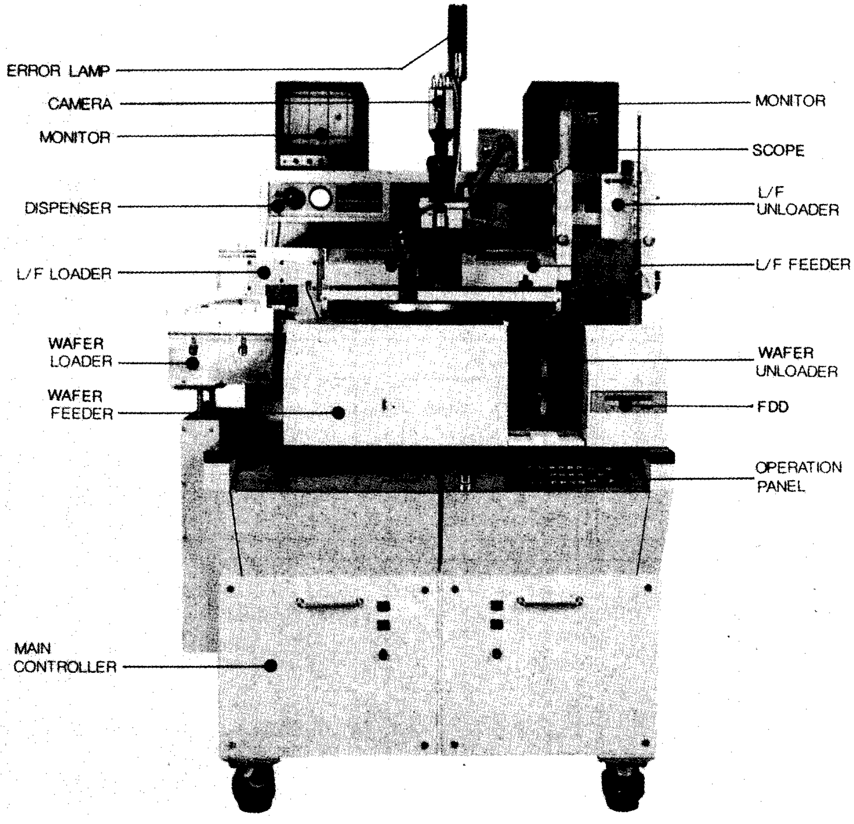

Fig. 1. Laboratory-developed semiconductor die bonder machine.

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actuated by five step motors, two DC motors, and five pneumatic cylinders. The lead frame stacked up initially in the frame loader is fed by the frame feeder and two mechanical clampers. When it is positioned at a bonding point, it is fastened by a window clamper. After bonding a die, the lead frame is unloaded and stacked in the lead frame container, called the frame stacker.

The overall control system is organized essentially as a concurrent multifunctional system, realized with multiple processors, where one central processor plays the role of the master and the other processors are the slaves. That is, the control system is designed to be a master-slave-type multiprocessor system in which the processors are tightly coupled. Each slave is a functionally dedicated system in software, and a time-shared common bus structure is utilized with a hardwired bus arbitration scheme [4].

The intercommunication is carried out by means of *semaphore* messages passed to a shared memory via the parallel bus architecture called the global bus (GBUS). The specific control system is shown in Fig. 2. The three 16-bit MC68000 microprocessors, which interface with the global bus, have the following designations: (1) the system master, called the supervisory controller (SUPC); (2) the visual pattern recognition unit (VPRU); and (3) the display unit (DISU).

In the system, numerous servomotors and actuators are controlled by the supervisory controller and sometimes by the other two units. The design of the servo control mechanism was carried out in a conventional way, so the presentation here will describe the supervisory controller and the vision subsystem.

Structured Supervisory Controller

The primary requirement in the design of the supervisory controller is that it must be capable of effectively coordinating tasks assigned to each slave. A secondary requirement is that it also provides user-friendly human-machine interfacing capabilities to operators in order to reduce errors and system setup time. Furthermore, a self-diagnosis function should be included in the supervisor so that the assembly machine can be maintained easily. In order to accommodate these requirements, the supervisor is designed with six function states: (1) idle state, (2) parameter state, (3) adjust state, (4) autoassembly state, (5) diagnosis state, and (6) emergency state.

In the *idle state*, the supervisor receives operational commands by letting the DISU display the main menu after initialization of the hardware. In the *parameter state*, various parameter values can be input and modified to describe the component characteristics for the control system. In the *adjust state*, each slave is capable of precisely tuning the motions of actuating motors interfaced to the slave. This helps human operators in heuristically choosing data that may be required for reliable visual signal processing. In the *autoassembly state*, the supervisor performs its own tasks and also assigns necessary tasks to each slave by monitoring the degree of completion of previously assigned tasks. In the *diagnosis state*, the supervisor first checks microprocessor-related hardware modules and then makes the DISU display current on-off states of all sensor/actuator signals. This permits human operators to monitor malfunctions of the sensors. Finally, in the *emergency state*, the supervisor shuts down all the motors/actuators to de-

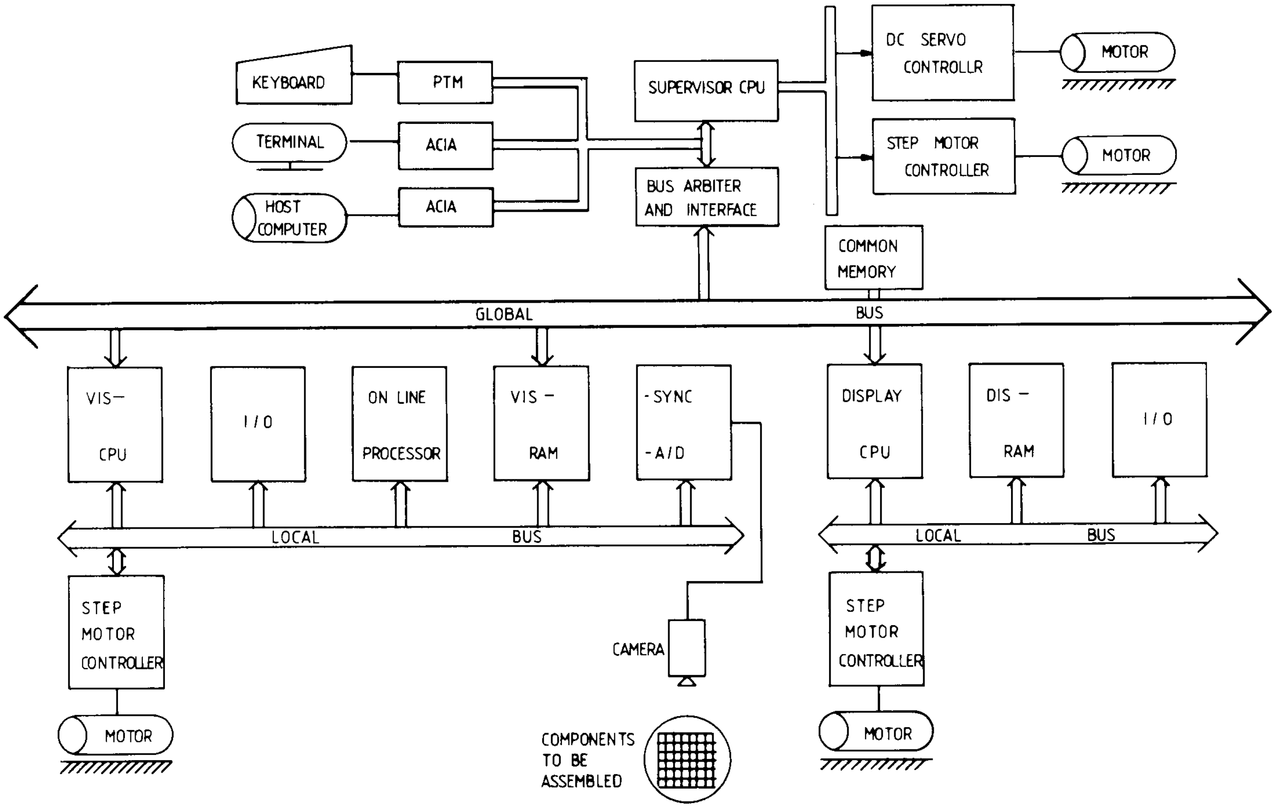

Fig. 2. Overall system configuration.

termine which limit switches are turned on outside the operating range.

The supervisor is designed as a multilayered structure type similar to the UNIX operating system [5]. That is, in the core of the supervisor resides virtually all the system hardware, such as AC motors, DC motors, step motors, limit switch sensors, pneumatic solenoids, and digital-to-analog (D/A) and analog-to-digital (A/D) converters. Thus, the supervisor can indirectly control and monitor all the hardware with the help of the slaves. In the next layer, there are software procedures for driving system hardware corresponding to the kernel of the UNIX. The outer layer, next to the kernel, is called the *function layer*, and includes primitive actions of the supervisor as well as those of each slave. The number of primitive actions for the semiconductor die bonding is about 150, which includes 70 for the supervisor and 40 for each slave. The outermost layer consists of the six functional states described previously. Because of its flexibility and modularity, the supervisor of such multilayered structure can be easily modified and expanded when other system functions must be added.

The supervisor tasks are divided into foreground and background. Background tasks are performed periodically according to a 10-msec timer with interrupt request. The supervisor checks each keyboard input command and then puts it into one of three command queues according to its task priority. The supervisor also checks error flags, and if the error flag is set, it resets the system. Otherwise, it reads and monitors the status of each slave.

Foreground tasks, on the other hand, are the main tasks performed in each state. First, the supervisor chooses a task to perform from the command queue with the highest priority. Next, the supervisor assigns the task to the predesignated slave via the shared memory. In our system, *system reset* and *emergency stop* are included in the highest priority group, and vision-related tasks, such as *binary image display* and *display of bonded die number*, are included in the next priority group. Almost all other jobs belong to the lowest priority group.

To ensure that the global bus is used only by one processor at a time, a hardwired bus arbitration is employed, while a *semaphore* message is utilized to avoid overwriting [2].

Visual Pattern Recognition

Before automatic assembly tasks can take place, the position and orientation of the components must be measured in real time, and each component must be inspected to determine if the component is a good die. The visual pattern recognition system is designed with a fast processing capability to perform these functions. Specifically, as the image memory for one frame, a new type of frame grabber has been designed by employing the TMS4161, a dual-ported dynamic random access memory (RAM) [6], and an on-line processor, which includes digital binarization circuits and double window counters specially designed to process images in real time. Furthermore, image processing software that is relatively insensitive to noise has been developed by employing a thresholding method based on a separability concept [7], Hough transform method [8], projection method, and edge preserving smoothing algorithms [9], with some modifications.

Video-Rate Frame Grabber

To discretize a video frame with 256 × 256 resolution at the rate of 60 times per second, the horizontal analog video signal was converted to an 8-bit digital signal with a 156-nsec sampling time. In this case, the sampling time is shorter than the response and/or access time of a typical dynamic or static RAM. This means that conventional memories cannot be used for the video-rate frame grabber. To resolve this problem, a dual-ported dynamic RAM was adopted, the TMS4161. The most interesting feature of the TMS4161 is that 256 shift registers with fast access time are connected to the conventional 64K-bit dynamic RAM in parallel. Thus, in the TMS4161, digitized visual image data are first stored in the serially connected 256 shift registers, and then 256 bit image data stored in the 256 shift registers are transferred to the dynamic RAM within 500 nsec. Thus, only 500 nsec is required to use the dynamic memory to store a line of data per every 63.5 μsec. This enables the central processing unit (CPU) to use the video memory for other purposes. However, there is some difficulty in using the TMS4161 due to three different types of addressing required by the CPU, refreshment, and the line generator. This difficulty was resolved by employing an 8203 dynamic RAM controller, which can arbitrate the addressing requirements of refreshment and CPU. Finally, to design the multiplexer and arbiter for the addressing requirement of the CPU and line generator, a 26-to-16 multiplexer is used and the necessary logic circuits for the arbiter are devised by considering the arbitration algorithm and by utilizing the 82S129 programmable read-only memory.

On-Line Preprocessing Unit

The visual pattern recognition for the component assembly can be divided into off-line processing and on-line processing. With off-line processing, process parameters should be determined with high precision, including the threshold value for binarization, angle of orientation, size of the components, and the number of image pixels corresponding to the minimal movement of the *XY* table.

On the other hand, with on-line processing, quality inspection is performed for each object and calculations are made of positional deviations from the prespecified pickup position. Thus, some preprocessing algorithms for the on-line function must be implemented by hardware circuits for fast data processing. This specific hardware is called the *on-line processing unit* in our system.

The on-line preprocessing unit is composed of digital comparators to make the gray-level image into the binary image by means of threshold value, window and line counters, and the interrupt requester. Here, the window counters play the role of counting the number of black pixels in a line, where the number of black pixels in the windows will be used in quality inspection and in determining positional deviations. Hardwired window counters reduce on-line processing time.

Thresholding Algorithm

For the semiconductor die bonding machine, the three objects that constitute the wafer are the rectangular shape of semiconductor dies, kerfs, and the metal base. Here, *kerf* is a channel between the semiconductor dies. The gray-level image of the wafer is binarized in such a way that the metal base and semiconductors become white images and kerfs become black images. The brightness of the semiconductors versus the kerfs is slightly different, and the brightness of the semiconductors versus the metal base is quite different. Thus, binarization by a single thresholding value will not succeed. In addition, the histogram of the image is quite noisy.

To resolve these difficulties, a thresholding method using the concept of a separability function [7] is employed here, and the result is found to be robust when compared to other methods. The method is first applied to the image to determine the threshold value that discriminates the metal base from the other objects. Then the whole image is modified so that those objects whose gray levels are greater than the threshold value are temporarily eliminated. The threshold method is then reapplied to the modified image to determine a second threshold value, which can discriminate between silicons and kerfs. Experimental results on the binarization by the proposed threshold method are shown in Fig. 3.

Measurement of Component Size

To use the windowing technique for fast image processing, it is necessary to measure accurately the size of the component, i.e., the die size. For this, the binarized wafer image is utilized along with the rectangular die image. The binarized wafer image is first projected in both the horizontal and vertical directions. Since the projection implies the integration of the intensity of all pixels in a specified direction, effects of noise due to quantization and incomplete threshold should be eliminated. Then two peak values are found from the one-dimensional projected data by application of the edge preserving smoothing method [9], which reduces the component size error due to the nonconstant width of kerfs in the binary image. Experimental results on the proposed measurement technique have proved to be satisfactory, as shown in Fig. 4.

Measurement of Component Orientation

Since the object is rectangular, the boundary of the object is a straight line. Thus, to measure the orientation of the component, it is sufficient to obtain the line equation for one of the boundary line segments. To reduce the processing time, we put a window on the upper region of the component and calculate the corresponding line equation. Specifically, the Hough transform method [8] is used to calculate the line equation, and then the orientation is calculated from the line slopes. Experimental results using the proposed method are shown in Fig. 5. The processing time of the proposed method appears to be less than the Stanford Research Institute (SRI) method [10] and the conventional Hough transform method without a window.

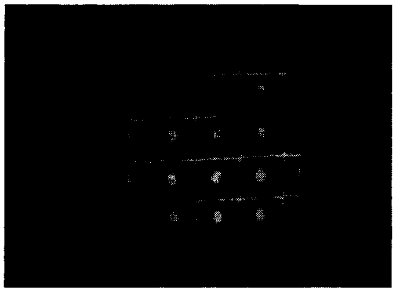

Fig. 3. Binary image resulting from thresholding.

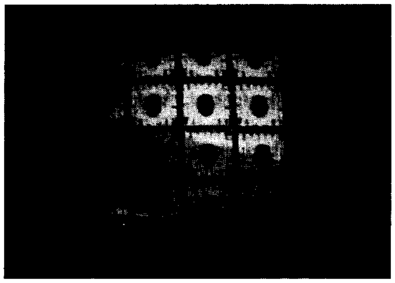

Fig. 4. Experimental results of size measurement.

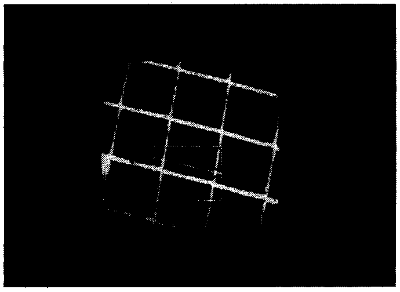

Fig. 5. Experimental results of orientation measurement.

Quality Inspection and Calculation of Positional Deviation

Before assembling, the quality of the component should be checked. In the case of die bonding, quality inspection means checking whether an *ink dot* is marked on the central region of the die. In order to improve the processing speed of the inspection, an additional hardware window is devised corresponding to the marking position of predetermined size so that the inspection can be done through comparison of this window with the binarized component image.

The final step is the calculation of the positional deviation of the component from the predetermined position. The projection method is again applied to the window binary image, as shown in Fig. 6. This deviation is corrected by driving the motors for the *XY* table in the servo system, and finally the die is picked up and bonded by the bonding head.

Display Unit

The display unit is composed of a camera interface, a set of double buffer memory, called *vision RAM* and *display RAM*, and a display processor for real-time (i.e., 63.5 μsec) display of die image, message, and graphic patterns, such as lines, circles, and characters.

For camera interface, a real-time image digitizer has been designed and implemented. For pattern generation, algorithms have been developed for generating lines and circles as well as characters. For display on the monitor, D/A conversion and the SYNC

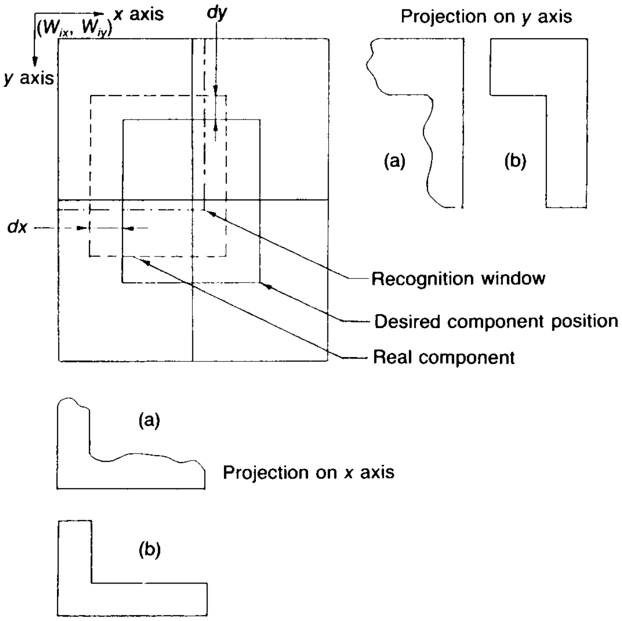

Fig. 6. Measurement of positional deviation.

(synchronizing signals) mixer are implemented. Since the on-line display occupies only a small fraction of the display processor time, some of the servo mechanism control was performed by this display processor.

Concluding Remarks

The design has been outlined for the control system for automatic assembly of microelectronic components. The system consists of a structured supervisory controller, a visual inspection/measurement subsystem, an information display subsystem, and a servo subsystem. The proposed system is flexible and reliable due to modular design and the structured supervisor with diagnosis capability. The system minimizes manual operation via automatic measurements and correction of object orientation and component size with the aid of a vision system.

The proposed control system was implemented and applied to a lab-type semiconductor die bonding machine and successfully tested in real time. In the test, we were able to reduce the bonding cycle time to 0.8 sec/die (0.8–7.0 mm^2 sized die) with the system presented here.

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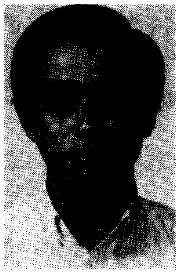

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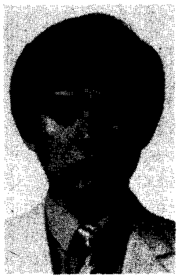

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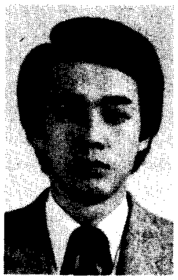

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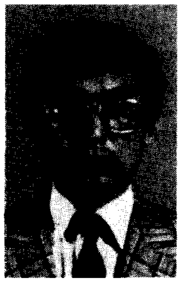

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