calculations) are less than 1%. Formulae are very simple to evaluate and do not require extensive computer calculations.

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FAST LINE DETECTION ALGORITHM USING MULTIVALUED IMAGE CODING

Indexing terms: Image processing, Pattern recognition

A fast vision algorithm is proposed for detecting geometrical features such as line slopes of a polygonal object by using a multivalued image. Based on the fact that the multivalued image holds the local topological property of the original binary image, the algorithm extracts features by simple summation of weighted values of pixels in the multivalued image. Owing to the fact that the algorithm is easily implementable in hardware, its performance is experimentally shown to be very efficient in comparison with those of other methods.

Introduction: The use of machine vision in automation systems is continually increasing for enhanced flexibility and intelligent operation. For object pattern recognition and classification, various image processing algorithms, including chain coding or run length coding, have been suggested for machine vision systems. While it is natural to seek more advanced algorithms that are applicable for more general scenarios, many of existing algorithms can be very inefficient for certain perception tasks involving simple-shaped objects, requiring considerable computation time. Recalling that, for a higher production rate, the vision system in manufacturing is usually required to process visual data as fast as possible, we may note that it is also important to seek task-specific algorithms even if the scope of application is somewhat limited. In the electronics industry, inspection and assembly of simple-shaped components are important automation tasks, and unorthodox vision methods can be employed. In this regard, we have reported[1] that the Hough transform (HT) technique for line detection is very effective and efficient for die-bonding machines, which are a small electronic component assembly machine used in semiconductor manufacturing.

In this letter, a vision algorithm that is faster than Hough transform is proposed for detecting geometrical features such as line slopes of a polygonal object by using the notion of a multivalued image (MVI).[2] The proposed algorithm is based on the observation that each pixel in the multivalued image has the local topological property of the original binary image. The algorithm, which extracts features by simple summation of weighted pixel values in MVI, is easily implemented in hardware. The performance of the proposed algorithm is experimentally compared with those of the Hough transform method[3] and the least square error (LSE) fit.[4]

Line detection using multivalued image coding: Let there be a given preprocessed binary image, consisting of $M \times N$ pixels, and let the location of a pixel be denoted as (x, y) with x and y being positive integers such that $0 \leq x \leq M-1$ and $0 \leq y \leq N-1$, respectively. Let $F(x, y)$ be the value of a pure binary image, i.e., $F(x, y) \in \{0, 1\}$, and, referring to Fig. 1, define $f_i(x, y)$, $i = 0, 1, \ldots, 8$, as

$$\begin{aligned} f_0(x, y) &= F(x, y) \\ f_1(x, y) &= F(x+1, y) \\ f_2(x, y) &= F(x+1, y+1) \\ f_3(x, y) &= F(x, y-1) \\ f_4(x, y) &= F(x-1, y-1) \\ f_5(x, y) &= F(x-1, y) \\ f_6(x, y) &= F(x-1, y+1) \\ f_7(x, y) &= F(x, y+1) \\ f_8(x, y) &= F(x+1, y+1) \end{aligned} \quad (1)$$

In eqn. 1, it is assumed that if either x or y takes a value outside the specified range in $0 \leq x \leq M-1$ and

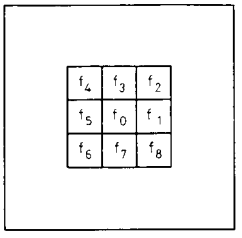

Fig. 1 $f_i(x, y)$
$i = 0, 1, 2, \ldots, 8$

$0 \leq y \leq N-1$, then $f_i(x, y) = 0$. Define a function $G(x, y)$, for $0 \leq x \leq M-1$ and $0 \leq y \leq N-1$, by the relation

$$G(x, y) = \left[\sum_{i=1}^{8} f_i(x, y) 2^{(i-1)}\right] f_0(x, y) \quad (2)$$

$G(x, y)$ is referred to as multivalued image,[2] abbreviated as MVI, because it consists of the binary value $F(x, y)$ and its eight neighbourhood values. For each (x, y), note that the transformation in eqn. 2 transforms a one-bit binary number into an eight-bit binary number, and thus $G(x, y)$ can be considered to be an eight-bit binary number with $f_0 f_1$ being the least significant bit and $f_0 f_8$ the most significant bit.

Comparing $F(x, y)$ with $G(x, y)$, we may say that $F(x, y)$ simply represents the local image value at (x, y) while $G(x, y)$ shows the local topological property or pattern at the neighbourhood of (x, y). For certain feature detection such as the slope of a line, we shall show that, instead of examining the totality of $F(x, y)$, information obtained by processing $G(x, y)$ in an appropriate manner can be more efficient.

For notational simplicity, each of the eight-bit numbers $(b_8, \ldots, b_1)_2$, where $b_i \in \{0, 1\}$, is denoted as q_k with k being the decimal equivalent of the binary number, i.e.,

$$q_k = (b_8 b_7 b_6 b_5 b_4 b_3 b_2 b_1)_2 \quad k = 0, 1, \ldots, 255$$

$$k = \sum_{i=1}^{8} 2^{i-1} b_i$$

The, for each $k = 0, 1, \ldots, 255$, let $h(q_k)$ be the number of pixels in the image such that $G(x, y) = q_k$. Then, $h(q_k)$, $0 \leq k \leq 255$, constitutes the histogram of MVI.

Now an algorithm for detecting the slope of a line is proposed. The pattern of $G(x, y)$ for each q_k, $k = 0, 1, \ldots, 255$, is examined and the most suitable value w_k representing the line slope for the pattern is assigned. For example, consider the case of $q_{36} = (00100100)_2$ as shown in Fig. 2*a*. We can say that this pattern is most likely to be a line segment with slope 2, i.e., 63·4°. By the same reasoning, we can observe that

$q_{68} = (01000100)_2$ as in Fig. 2*b* is the portion of line with slope 90·0°. In Fig. 2*c* is shown the pattern for q_{66} with w_k = 63·4°. In this way, we can assign the characteristic value w_k for each q_k, $k = 0, 1, \ldots, 255$, as partially listed in Table 1. Then,

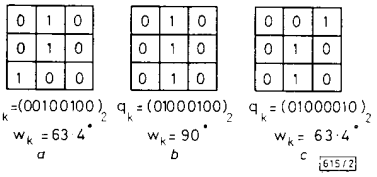

Fig. 2 *Examples of multivalued image coding and its weight*

Table 1 WEIGHTS FOR LINE SLOPE

q_k	w_k
0	0·0°
1	0·0°
...	...
36	90·0°
...	...
66	63·4°
...	...
68	63·4°
...	...
255	0·0°

by using the histogram of MVI and w_k, we can calculate the slope of the entire line as the value J given by

$$J = \left[\sum_{k=0}^{255} w_k h(q_k)\right] \Big/ \left[\sum_{k=0}^{255} h(q_k)\right] \quad (3)$$

J in eqn. 3 can be regarded as an average slope of the line. The procedure of the algorithm is depicted graphically in Fig. 3.

It is remarked that, if the values of some w_ks are not so obvious as that of, for example, w_{68} = 90·0°, one may adjust the values of w_ks in such a way that, for given standard patterns, the total error is minimum.

Experimental example: To show the validity of the proposed algorithm, the following experiment is conducted: Given an eight bit grey level image using a digitiser, analyse its histogram to get an appropriate threshold level for binarisation. With the acquired threshold level, the binary image is obtained and converted to MVI. This MVI is histogrammed by a histogramming hardware. With this histogram and precalculated w_ks, the host computer (MC68000) evaluates eqn. 3.

For example, for the line with slope 70.5° as in Fig. 3, we have obtained $h(q_k)$'s being zero except $h(q_{36}) = 35$, $h(q_{66}) = 46$ and $h(q_{68}) = 47$. With this histogram and w_{36}, w_{66} and w_{68} in Table 1, the evaluated slope using eqn. 3 is found to be 70·6°. In case of another real image of a line with 14·2°, we have obtained the slope to be 14·1° using eqn. 3. Further experimental results are shown in Table 2.

We have implemented the MVI algorithm and histogrammer in hardware and, by employing the hardware, line detection for a real semiconductor die image is performed. We

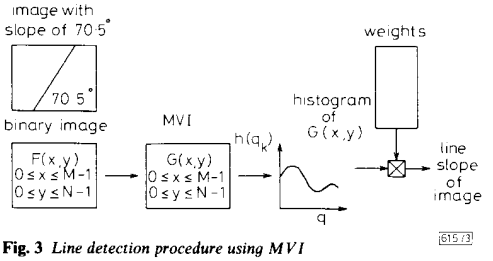

Fig. 3 *Line detection procedure using MVI*

find that the detection time is 58 ms and the absolute error average is 0·04°. When the Hough transform technique[3] is applied, the detection time is 16·8 s and the absolute error is 0·29°. The Hough transform technique, which is rather robust to noise and very efficient when the range of slope is known to be small (for example, ±5°), is not suitable for randomly-placed objects. We have also attempted to use least square error (LSE) fit[4] and obtained that the detection time is 599·6 ms and the absolute error average is 0·14°. To study noise immunity, we have added a Gaussian noise to '3 × 3 mean-filtered' grey level image, around the threshold level for binarisation. As shown in Table 3, the experimental results shows that the MVI algorithm is as good as HT and LSE methods in the case where the variance of the Gaussian noise is not greater than nine. When the variance is larger, the value of MVI is more randomised as the noise is added to the boundary of an object, and noise immunity is deteriorated. In an industrial manufacturing environment, the effect of image noise is reducible by well conditioned illumination.

Table 3 EXPERIMENTAL RESULTS FOR NOISY IMAGE

Noise variance	Computed slope, degrees		
	MVI	HT	LSE
0*	27·12	27·00	27·18
1	27·12	27·00	27·17
4	27·12	27·00	27·16
9	27·18	27·00	27·29
16	22·74	27·00	27·15

Real slope = 27·10°
* 0 means 3 × 3 mean-filtered image

Concluding remarks: It was shown that a weighted sum of the histogrammed multivalued image can be used to detect the slope of a line, and it was proved through experiments that the proposed method is faster than typical line detection algorithms since the algorithm can be easily implementable in hardware. Other geometrical features such as area and perimeter of an object can be easily computed in a similar manner by using MVI. For example, the area is the number of the

Table 2 EXPERIMENTAL RESULTS

Real slope, degree	Computed slope, degrees			Computation time, ms		
	MVI	HT	LSE	MVI	HT	LSE
0·45	0·47	0·00	0·62	58·5	16863·4	598·9
8·07	8·07	8·00	8·29	58·0	16853·6	599·0
27·10	27·12	27·00	27·18	58·4	16480·3	599·5
61·31	61·13	61·00	61·15	58·6	16428·1	598·6
−22·81	−22·75	−23·00	−22·80	57·5	16862·3	599·7
−38·16	−38·18	−39·00	−38·41	58·5	16480·3	599·5
−63·04	−63·04	−63·00	−63·17	58·4	16452·8	599·6
Absolute error average	0·04	0·29	0·14	Average computation time, ms		
				58·3	16631·5	599·3

pixels with value 1 in binary image, and thus a pixel in the binary image which has at least one of the eight neighbourhood is transformed to a nonzero value in MVI. Therefore the sum of the histogram of MVI except 0 means the area of an object image. It can also be easily shown that the boundary pixels of an object are converted to the number between 1 and 254 in MVI since internal ones are converted to 255 and external ones to 0. Thus the perimeter, which is the number of pixels on the boundary of object, is the sum of the histogram of MVI except 255 and 0. The value of w_k for area and perimeter are shown in Table 4. Since the MVI contains the

Table 4 WEIGHTS FOR AREA AND PERIMETER

Area	$w_k = \sum_{k=0}^{k=255} h(q_k)$ for all q_k
Perimeter	$w_k = \sum h(q_k)$ for $q_k \neq 0, 255$
	$w_k = 0$ otherwise

relationship between neighbourhood pixels, it can also be used to generate the chain code.[2]

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HYBRID 11 Gbit/s PARALLEL PROCESSING DECISION CIRCUIT USING SUBMICRON SILICON BIPOLAR ICs

Indexing terms: Bipolar devices, Silicon

The design and implementation of a submicron-silicon bipolar parallel processing master-slave D-type flip-flop decision circuit, operating at data rates as high as 11 Gbit/s is described. This is the fastest reported decision circuit for silicon bipolar technology. The ICs used in the hybrid circuit were fabricated using a 0·6 μm, non-polysilicon emitter technology, and mounted in a package employing coplanar waveguides.

Introduction: The performance of lightwave communications systems continues to increase at a rapid pace. Systems for the next generation SONET rate of 10 Gbit/s are under intense research worldwide.[1,2] High speed integrated circuit technologies will be essential for overcoming bottlenecks in electronics for these systems, and for providing the enhanced functionality, reliability, and cost reduction required for their practical implementation. Silicon bipolar technology has lately emerged as one of the most promising low-cost, high performance technologies for application in multi-gigabit/s lightwave communication systems. Silicon bipolar 1 : 2 demultiplexers[3] and 2 : 1 multiplexers[4] operating beyond 11 Gbit/s have recently been reported. The performance achieved by these circuits is a consequence of innovative device processing, accurate device modelling, and aggressive circuit design.

We report on the design and performance of a prototype parallel processing[5] decision circuit based on submicron silicon bipolar master-slave D-type flip-flop ICs and implemented as a hybrid integrated circuit (HIC). The record data rate of 11 Gbit/s represents a substantial improvement as compared with 8 Gbit/s silicon bipolar decision circuits using the same IC in a non-parallel architecture,[3] and indicates the potential of silicon technology for future generation SONET telecommunication systems. We also discuss the hybrid package which was specially designed to achieve this result.

Circuit design: A block diagram of the parallel processing decision circuit is shown in Fig. 1. The hybrid circuit was

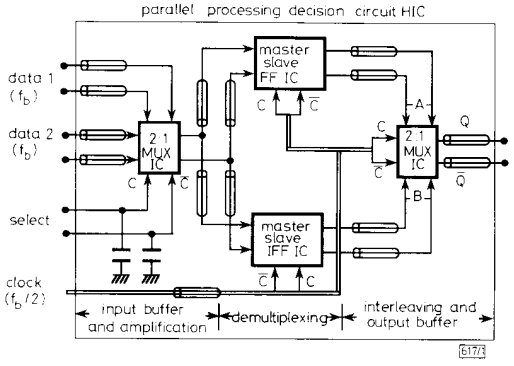

Fig. 1 *Block diagram of parallel processing decision circuit HIC*

constructed entirely from previously reported silicon bipolar decision circuits[3] and 2 : 1 multiplexers.[4] A multiplexer IC is used at the input as a differential amplifier to drive the two decision circuits and to improve the overall input sensitivity of the HIC. The multiplexer clock inputs are tied to DC control voltages, enabling steering one of the two inputs through the multiplexer to the decision circuits. The decision circuits are clocked at half the input data rate and in antiphase with respect to each other. As a result, each decision circuit demultiplexes and retimes alternating bits from the input sequence. This allows each decision circuit twice the time for bit regeneration, compared with a non-parallel architecture, giving a performance advantage to the parallel processing architecture (provided that the performance of the single decision circuit is limited by the internal toggle rate and not by the rise and fall times).

The decision circuits and multiplexers used in the hybrid circuit were fabricated using the Avantek ISOSAT™ silicon nitride self-aligned process which features 0·6 μm wide arsenic-doped emitters with 4 μm base to base pitch, deep trench isolation, 2 μm thick field oxide isolation, polysilicon resistors and a two layer TiW–Au metallisation.[6] The resulting transistors have a short circuit unity current gain frequency, f_T, in the range of 10–15 GHz, and a unity unilateral gain frequency, f_{max}, of approximately 20 GHz.

High performance packages have been designed for the hybrid circuit implementation of the parallel processing decision circuit. Two HICs were used. One HIC contains the front end amplifier and the two decision circuits. The other contains the recombining multiplexer. A short section of flexible coaxial cable connects the two circuits. This was possible since the ICs used in the hybrid circuits feature on-chip 50 Ω input terminating resistors to keep reflections to a minimum. Both hybrids utilise tapered coplanar waveguides